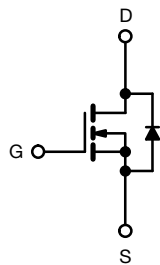
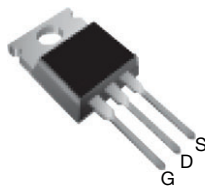


Power MOSFET

TO-220AB

N-Channel MOSFET

FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS*
Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

PRODUCT SUMMARY

V _{DS} (V)	1000
R _{DS(on)} (Ω)	V _{GS} = 10 V 5.0
Q _g max. (nC)	80
Q _{gs} (nC)	10
Q _{gd} (nC)	42
Configuration	Single

ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free	IRFBG30PbF
Lead (Pb)-free and halogen-free	IRFBG30PbF-BE3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V _{DS}	1000	V
Gate-source voltage	V _{GS}	± 20	V
Continuous drain current	V _{GS} at 10 V I _D	T _C = 25 °C 3.1 T _C = 100 °C 2.0	A
Pulsed drain current ^a	I _{DM}	12	A
Linear derating factor		1.0	W/°C
Single pulse avalanche energy ^b	E _{AS}	280	mJ
Repetitive avalanche current ^a	I _{AR}	3.1	A
Repetitive avalanche energy ^a	E _{AR}	13	mJ
Maximum power dissipation	T _C = 25 °C P _D	125	W
Peak diode recovery dV/dt ^c	dV/dt	1.0	V/ns
Operating junction and storage temperature range	T _J , T _{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^d	For 10 s	300	°C
Mounting torque	6-32 or M3 screw	10 1.1	lbf · in N · m

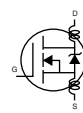
Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- V_{DD} = 50 V, starting T_J = 25 °C, L = 55 mH, R_g = 25 Ω, I_{AS} = 3.1 A (see fig. 12)
- I_{SD} ≤ 3.1 A, dI/dt ≤ 80 A/μs, V_{DD} ≤ 600, T_J ≤ 150 °C
- 1.6 mm from case

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	62	°C/W
Case-to-sink, flat, greased surface	R_{thCS}	0.50	-	
Maximum junction-to-case (drain)	R_{thJC}	-	1.0	

SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

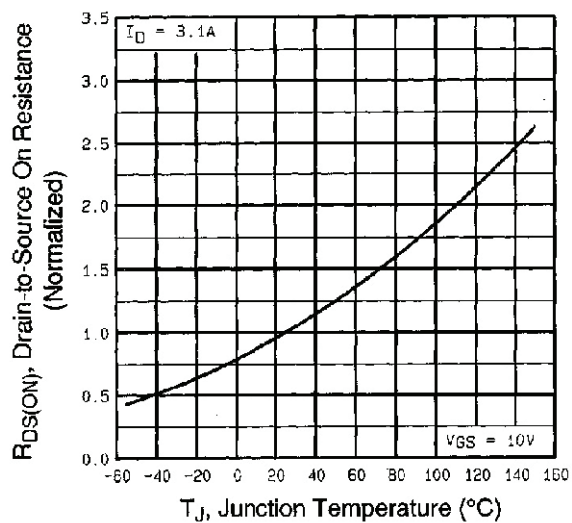
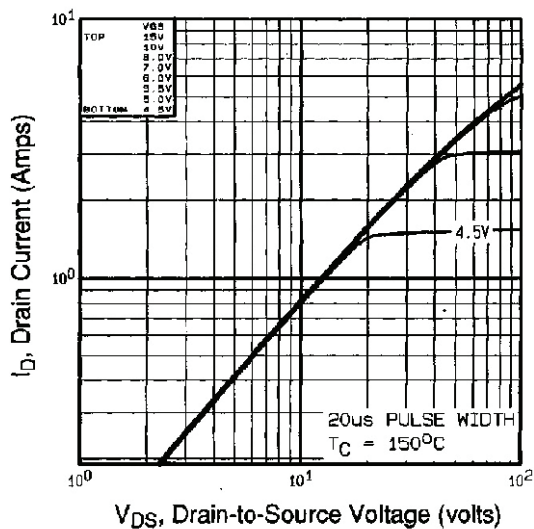
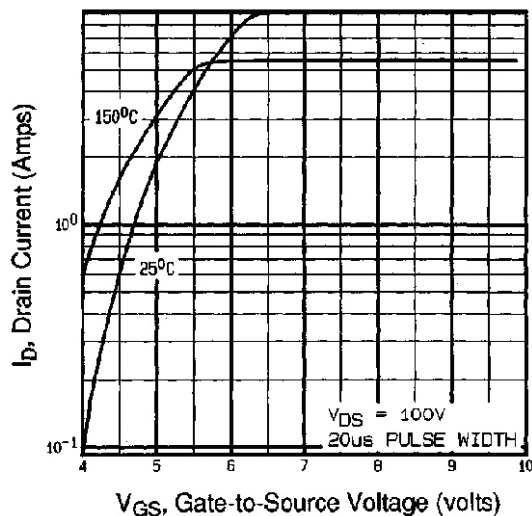
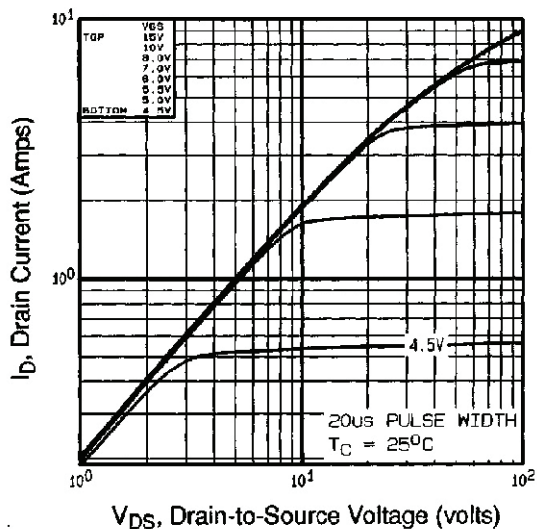
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$		1000	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$		-	1.4	-	V/ $^\circ\text{C}$
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-source leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 1000\text{ V}$, $V_{GS} = 0\text{ V}$		-	-	100	μA
		$V_{DS} = 800\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^\circ\text{C}$		-	-	500	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 1.9\text{ A}^b$	-	-	5.0	Ω
Forward transconductance	g_{fs}	$V_{DS} = 10\text{ V}$, $I_D = 1.9\text{ A}^b$		2.1	-	-	S
Dynamic							
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1.0\text{ MHz}$, see fig. 5		-	980	-	pF
Output capacitance	C_{oss}			-	140	-	
Reverse transfer capacitance	C_{rss}			-	50	-	
Total gate charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 3.1\text{ A}$, $V_{DS} = 400\text{ V}$, see fig. 6 and 13 ^b	-	-	80	nC
Gate-source charge	Q_{gs}			-	-	10	
Gate-drain charge	Q_{gd}			-	-	42	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 500\text{ V}$, $I_D = 3.1\text{ A}$ $R_g = 12\text{ }\Omega$, $R_D = 170\text{ }\Omega$, see fig. 10 ^b		-	12	-	ns
Rise time	t_r			-	25	-	
Turn-off delay time	$t_{d(off)}$			-	89	-	
Fall time	t_f			-	29	-	
Gate input resistance	R_g	$f = 1\text{ MHz}$, open drain		0.4	-	1.8	Ω
Internal drain inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal source inductance	L_S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	3.1	A
Pulsed diode forward current ^a	I_{SM}			-	-	12	
Body diode voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}$, $I_S = 3.1\text{ A}$, $V_{GS} = 0\text{ V}^b$		-	-	1.8	V
Body diode reverse recovery time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}$, $I_F = 3.1\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}^b$		-	410	620	ns
Body diode reverse recovery charge	Q_{rr}			-	1.3	2.0	μC
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\text{ }\%$



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



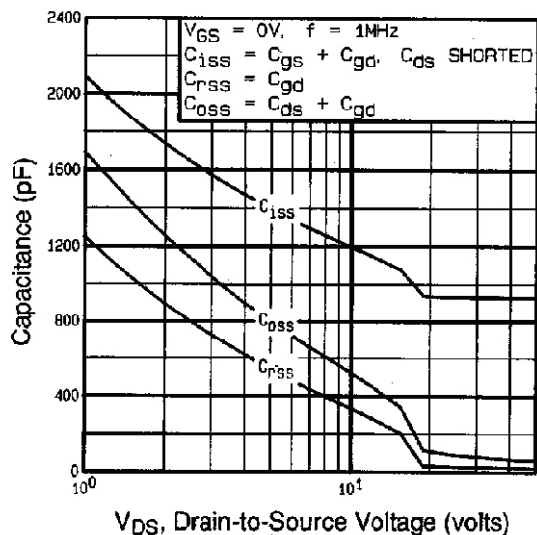


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

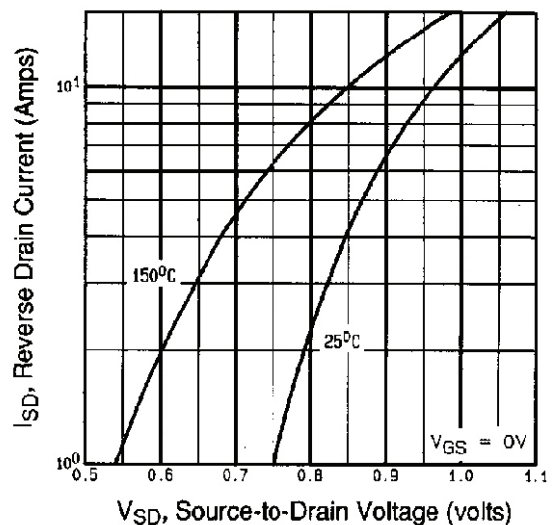


Fig. 7 - Typical Source-Drain Diode Forward Voltage

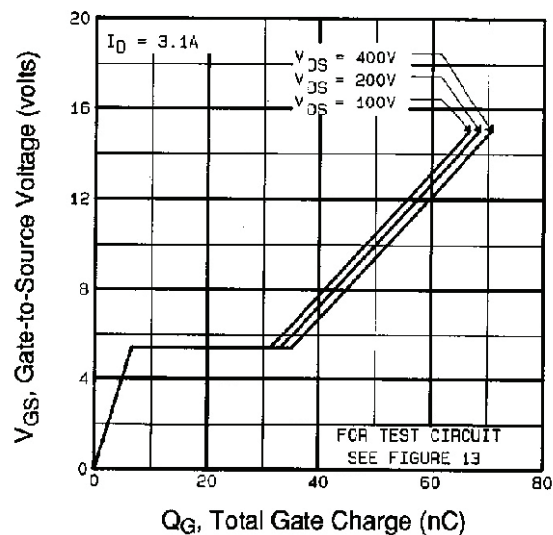


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

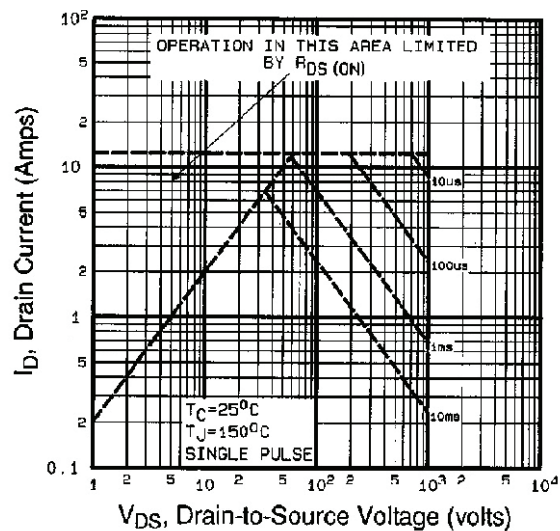
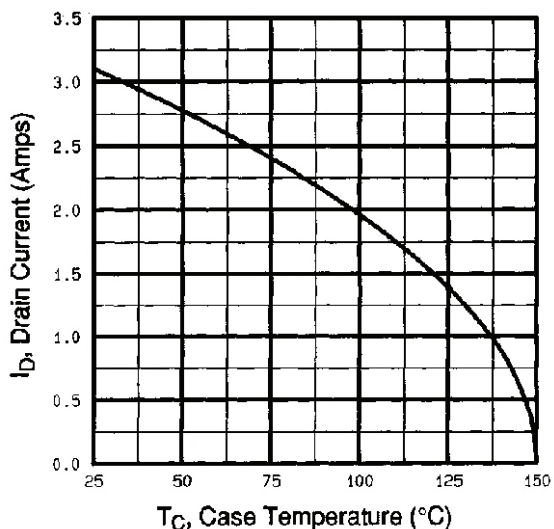
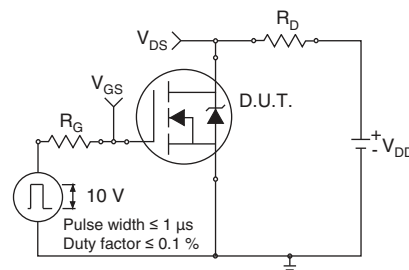
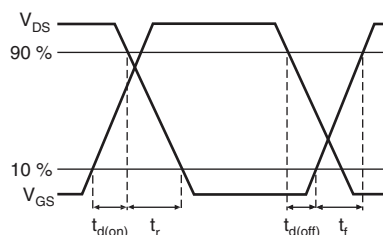
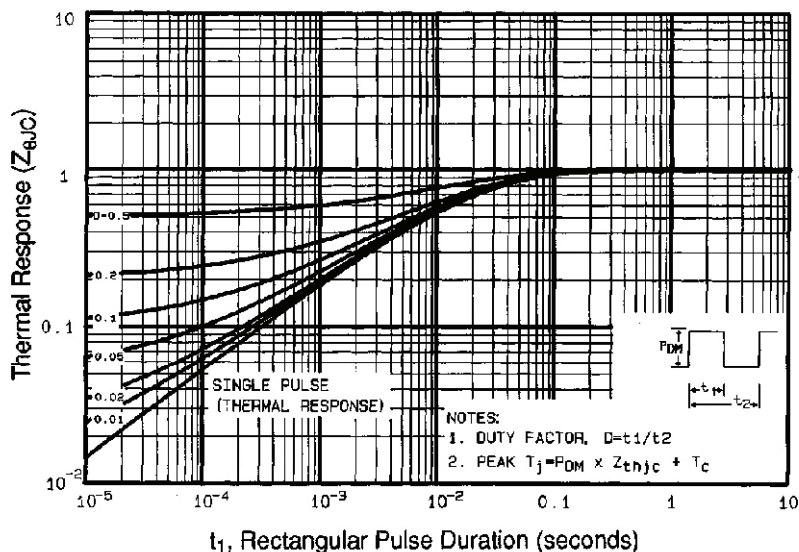
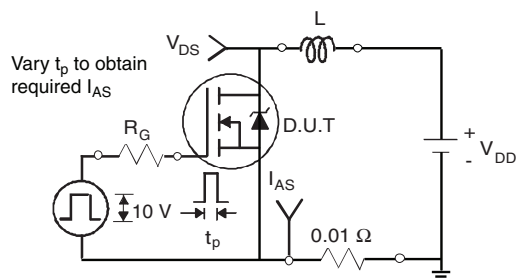
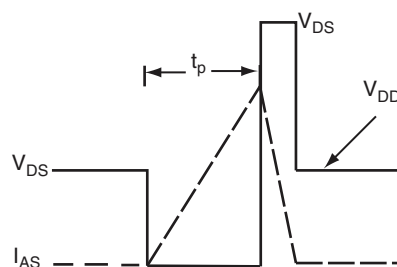


Fig. 8 - Maximum Safe Operating Area


Fig. 9 - Maximum Drain Current vs. Case Temperature

Fig. 10a - Switching Time Test Circuit

Fig. 10b - Switching Time Waveforms

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig. 12a - Unclamped Inductive Test Circuit

Fig. 12b - Unclamped Inductive Waveforms

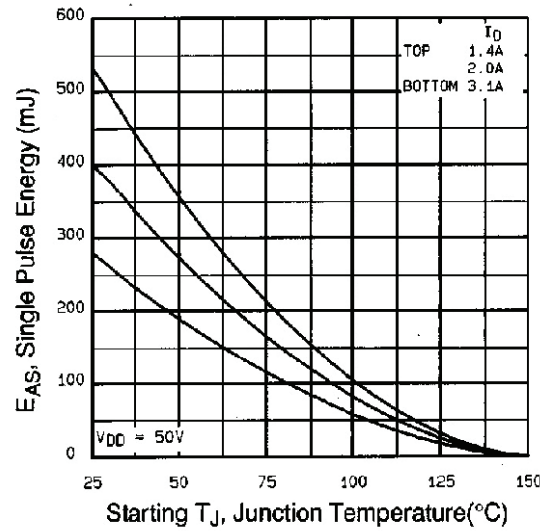


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

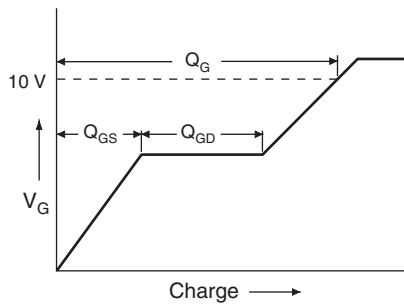


Fig. 13a - Basic Gate Charge Waveform

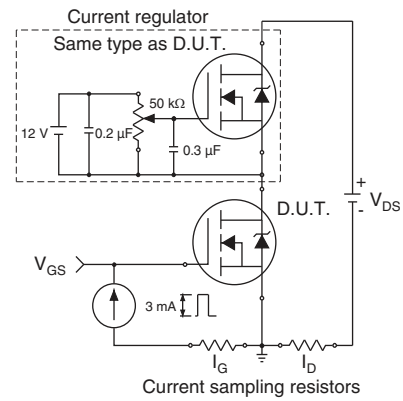
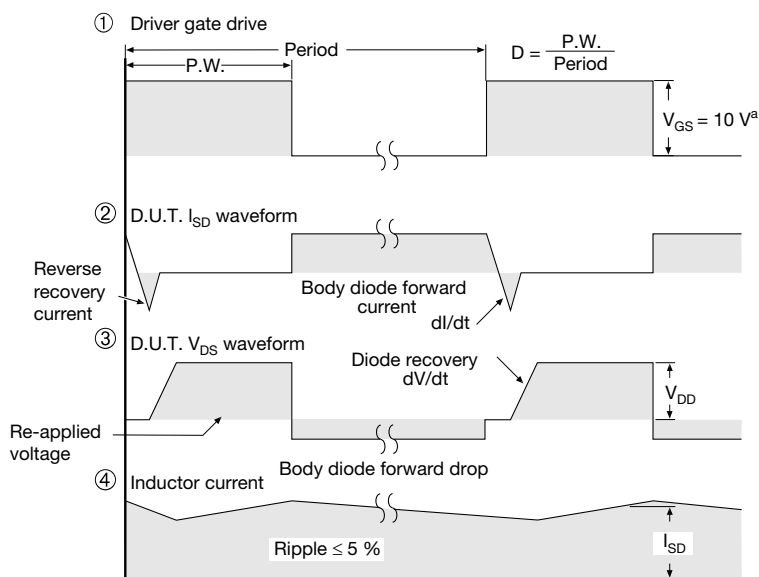
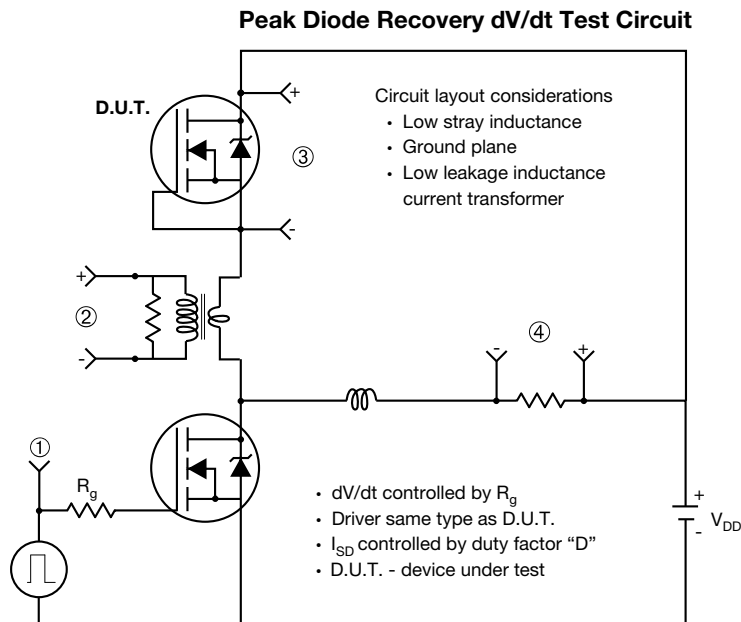


Fig. 13ab- Gate Charge Test Circuit



Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

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